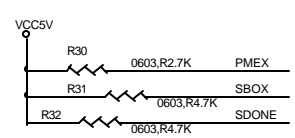
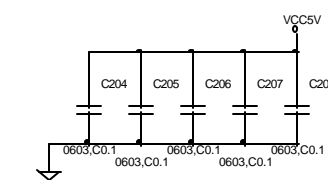
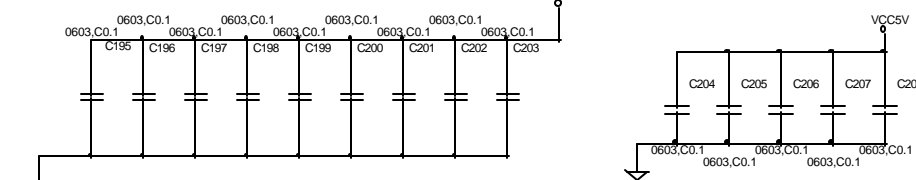
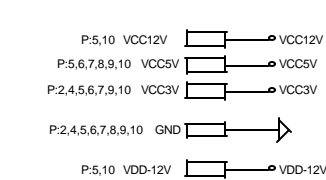
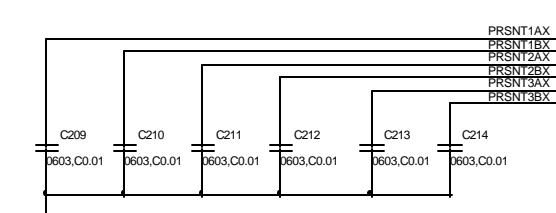
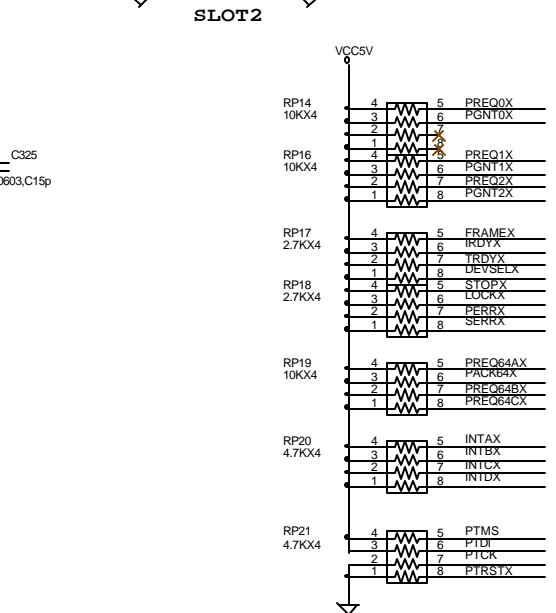
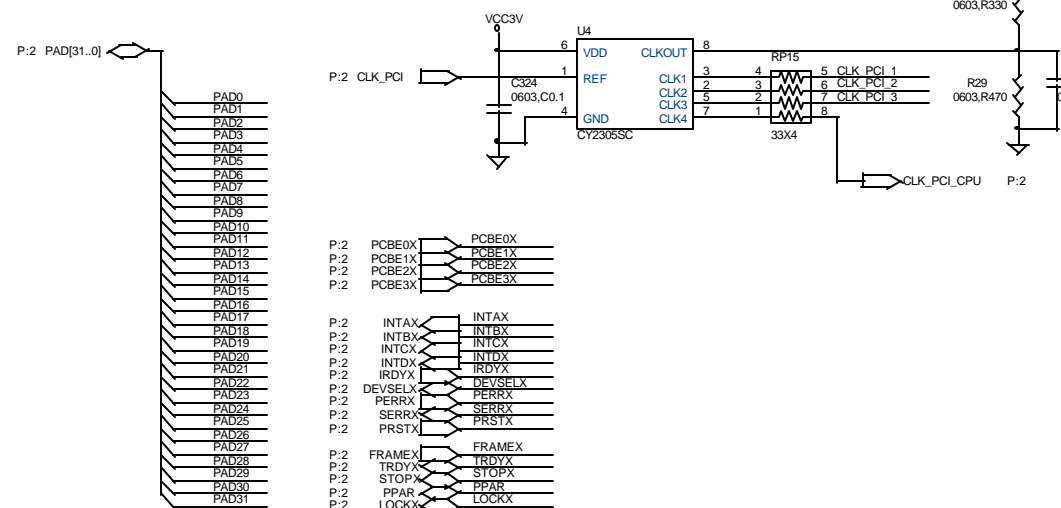
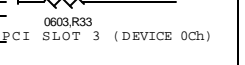
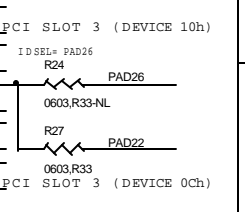
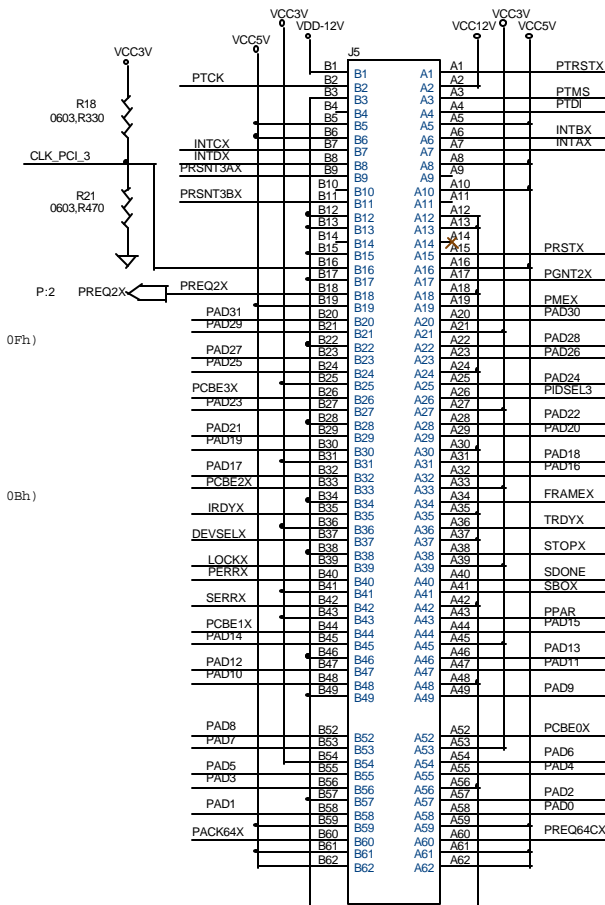
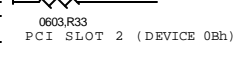
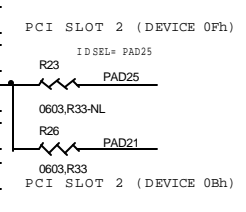
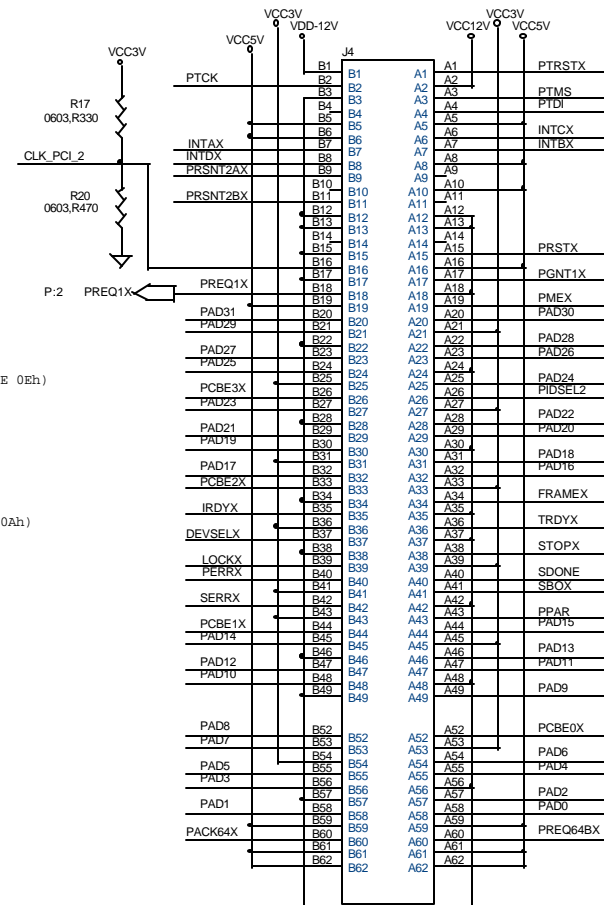
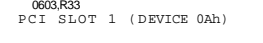
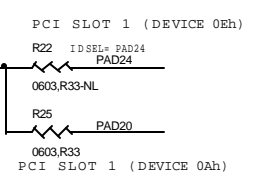
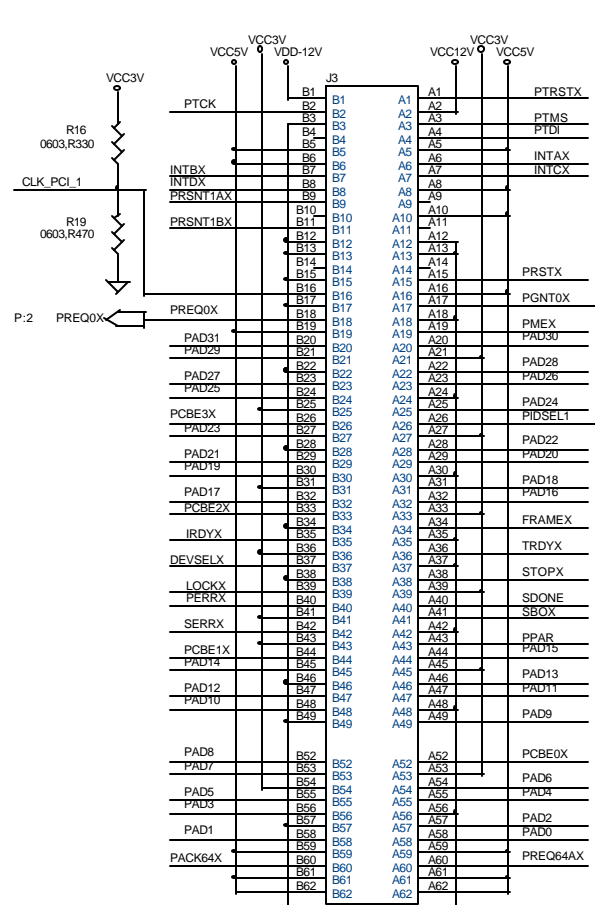


- P02 MACHZ
- P03 PCI CONNECTORS
- P04 SDRAM
- P05 ISA CONNECTORS
- P06 IDE & GPIO TEST
- P07 KBD, MOUSE, FDD, USB, ZTAG
- P08 SERIAL & PARALLEL PORTS
- P09 POSTCODE
- P10 POWER, RESET, FRONT PANEL

PRELIMINARY

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Drawn	Date	Title	Size	Document nr	ZF nr
K. Kevall		MACHZ EVALUATION 1: MAIN	C	9000041303	9400-0038-03
Checked		Designed by	Date	Friday, May 05, 2000	Sheet 1 of 11
		PPACKX			
		PPERRX			
		PPPE			
		PPSLINRX			
		PPSCLT			
		PPAFDRX			
		PPINITRX			
		PPBUSY			
		SCL			
		SDA			

BD1
8800-0038-03
PCBOARD



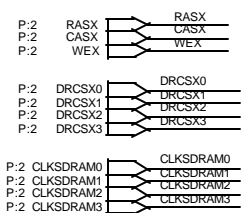
ZF Embedded, Inc.			
1052 Elwell Court Palo Alto, CA, 94303 (650) 965-3800			
Title: PCICONS			
Size: C	Document nr: 9000041303	ZF nr: 9400-0038-03	Rev: 3
Date: Friday, May 05, 2000	Sheet: 3 of 11		

DIMM0

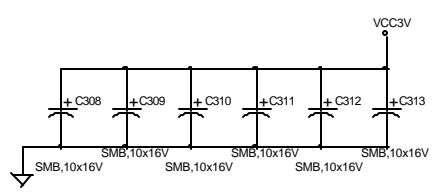
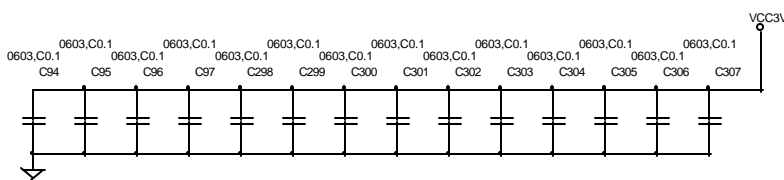
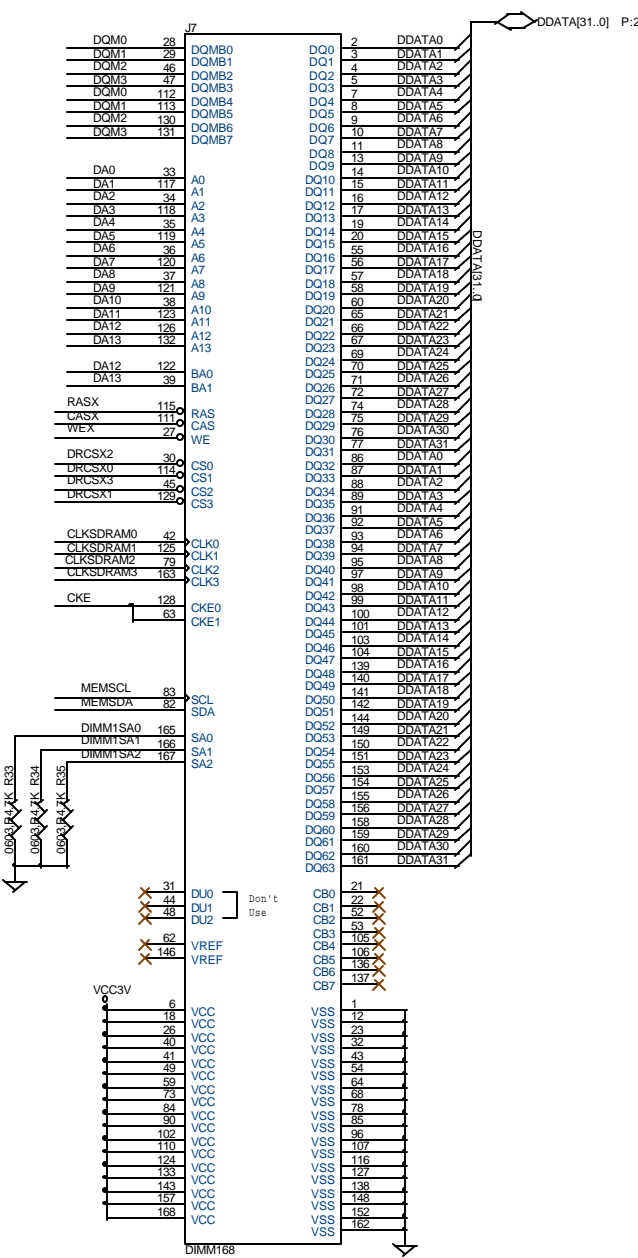
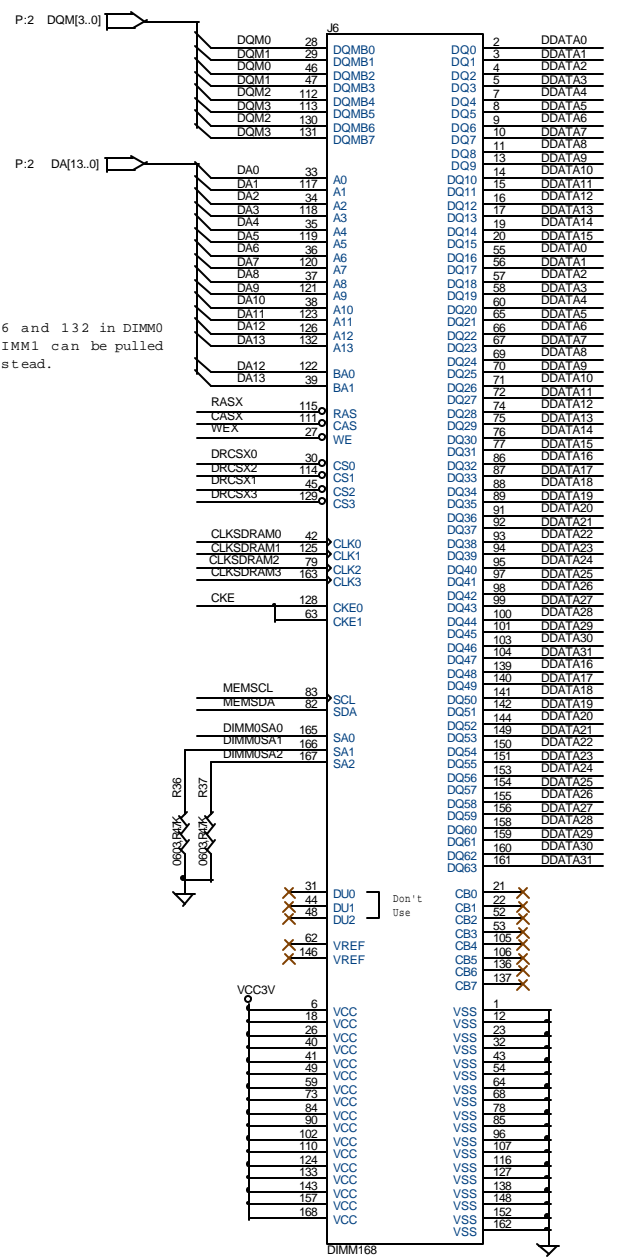
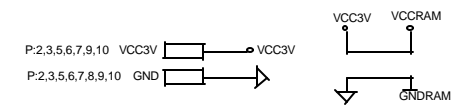
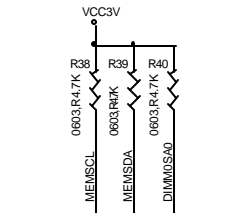
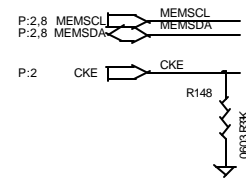
WITH STANDARD CHIP SELECT ROUTING

DIMM1

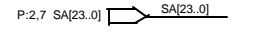
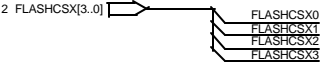
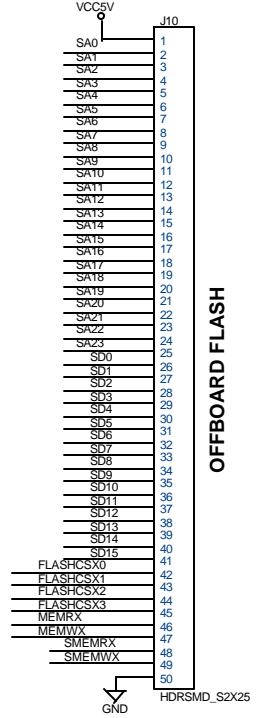
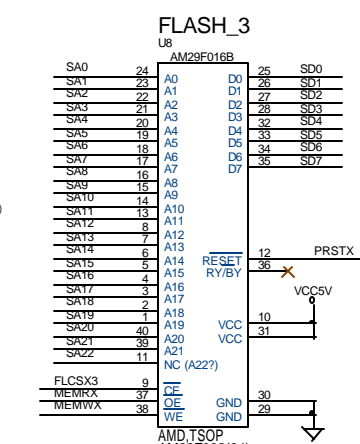
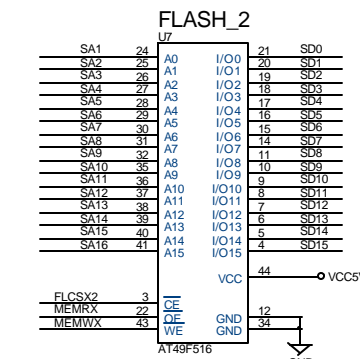
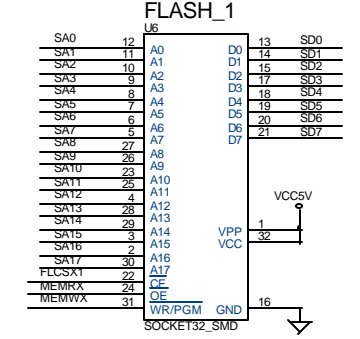
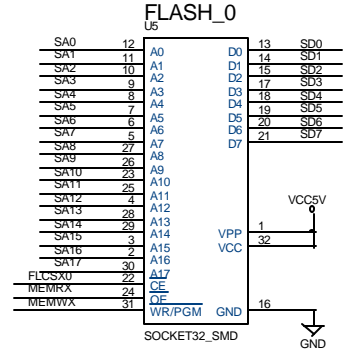
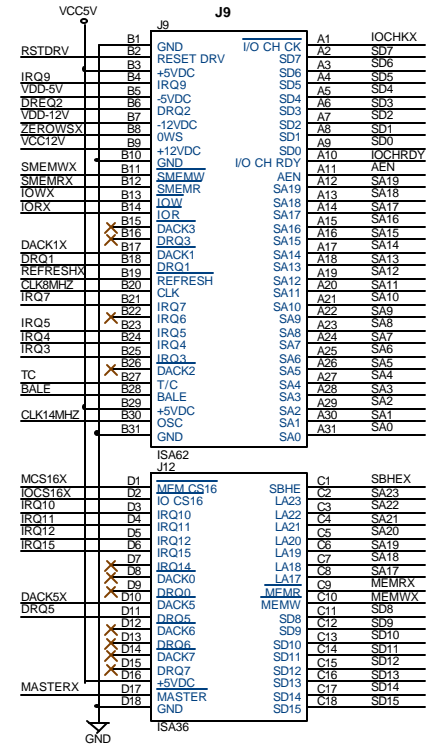
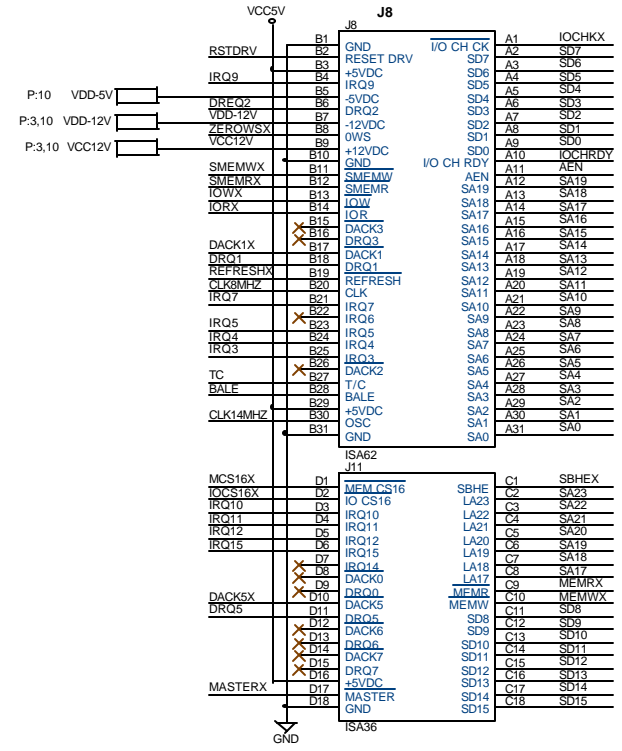
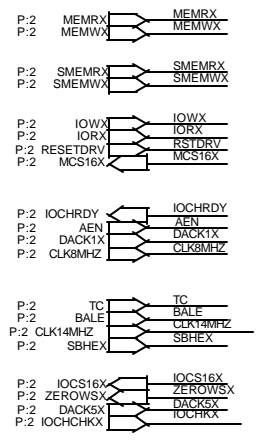
WITH ALTERNATIVE CHIP SELECT ROUTING



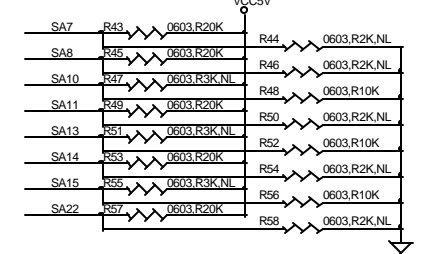
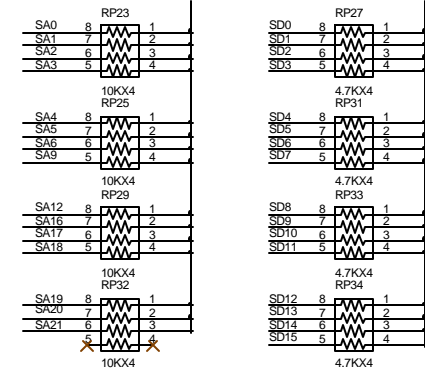
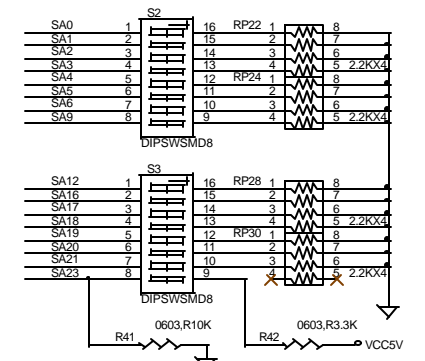
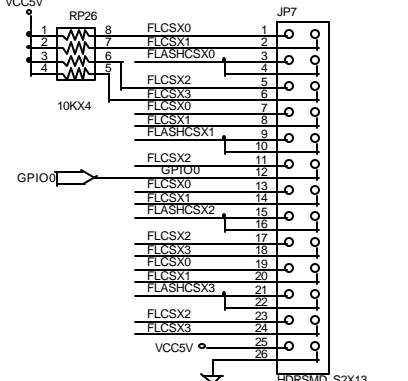
Pin126 and 132 in DIMM0 and DIMM1 can be pulled up instead.



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Title: SDRAM			
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Date: Friday, May 05, 2000		Sheet: 4 of 11	

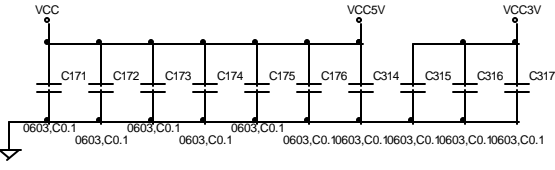
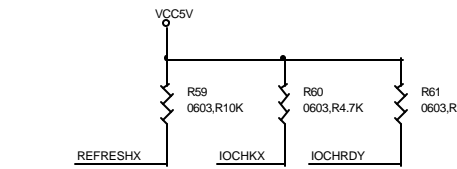
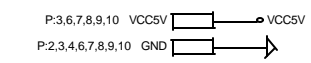
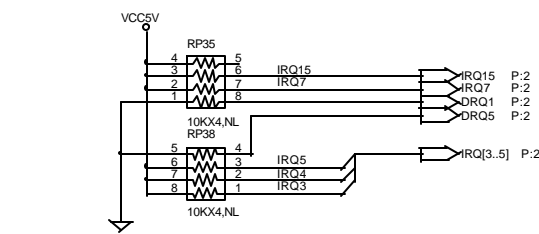
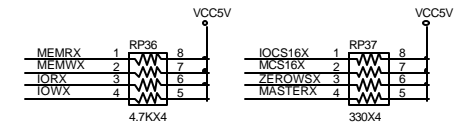


FLASH 0-4 CS CONF



MACHZ DEFAULT BOOTSTRAP VALUES - WITHOUT PULL-UPS/PULL-DOWNS

reset regs	value	description
23: BUR enable	1'b0	(BUR Disabled)
22: zfl enable	1'b1	(ZF Logic Enabled)
21: usb test mode enable	1'b0	(No USB Test)
20: back pci clock source	1'b1	(Use internal source)
19: back pci clk div	1'b0	(Divide sysclk_c by one)
18: front pci clk div	1'b0	(Divide sysclk_c by one)
17:16 1486 clk mode	2'b11	(3x sysclk_c)
15:13 1486 clk delay	3'b010	(factory default)
12: boot rom width 8/16	1'b1	(8 bit external ISA ROM)
11: int/ext bur	1'b1	(Use internal BUR when Ztag enabled)
10: SIO test mode	1'b0	(Test mode disabled)
09: Third PCI req/gnt enable	1'b0	(Third PCI req/gnt disabled)
08: 486 raw clock disabled	1'b1	(486 raw clock disabled)
07: 486 DLL enabled	1'b1	(486 DLL clock enabled)
06: Derive 32KHz from 48MHz	1'b0	(Using ext 32KHz Crystal)
05: Derive 14MHz from 48MHz	1'b0	(Using ext 14KHz Crystal)
04:0	1'b0	(User defined)

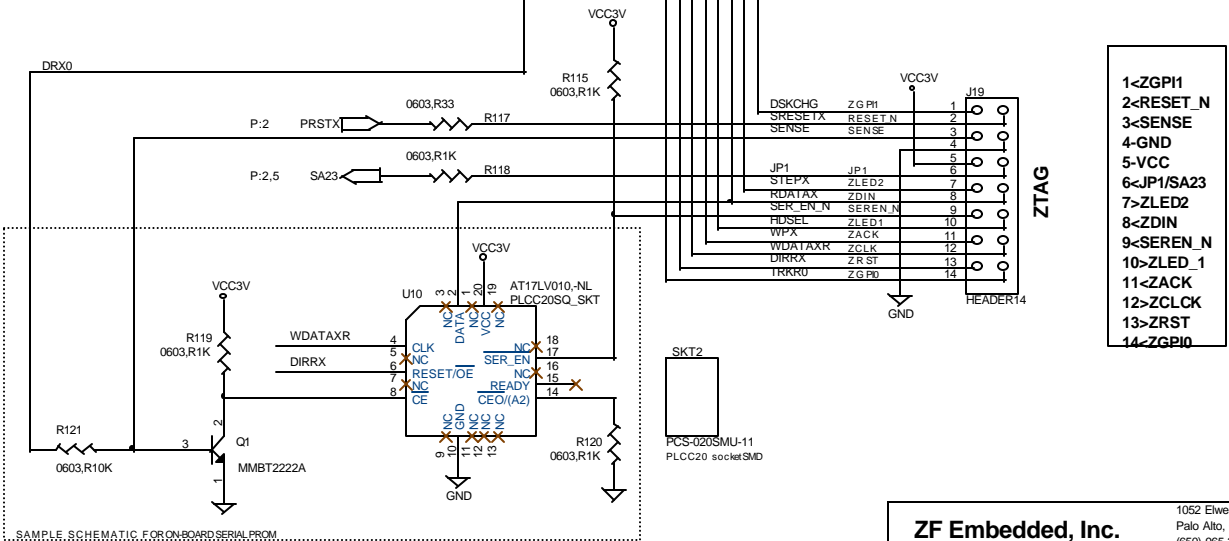
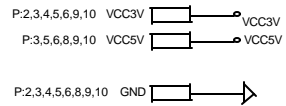
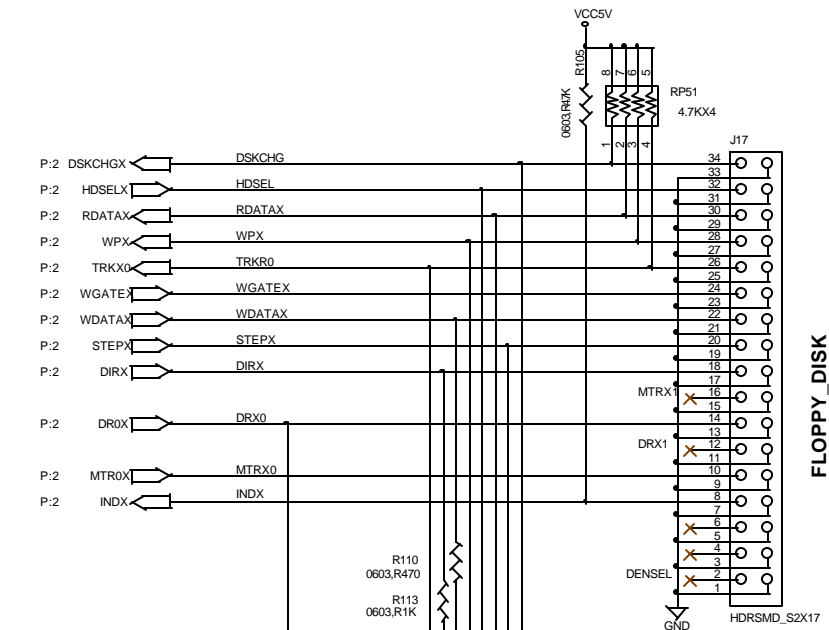
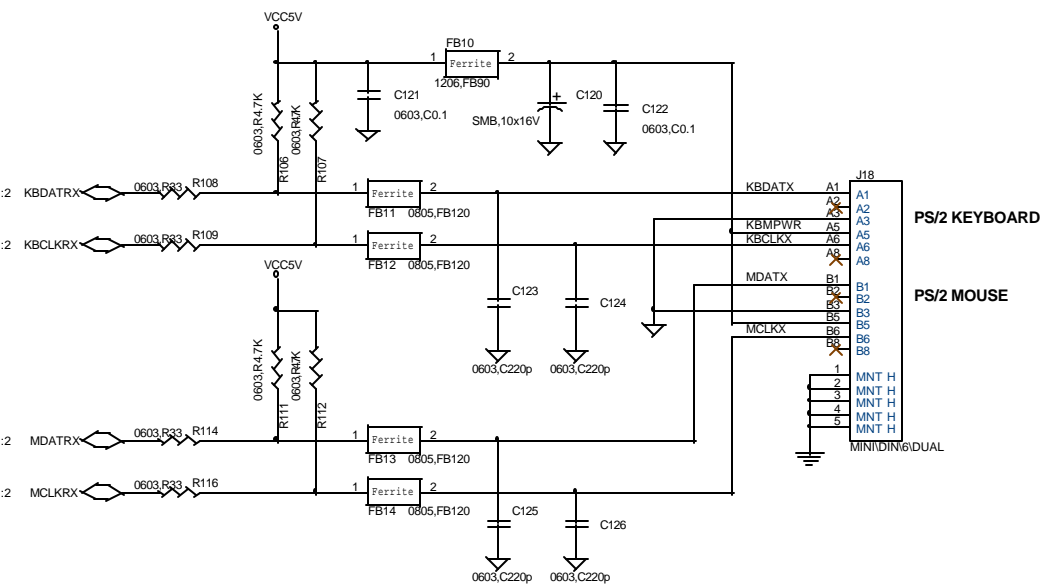
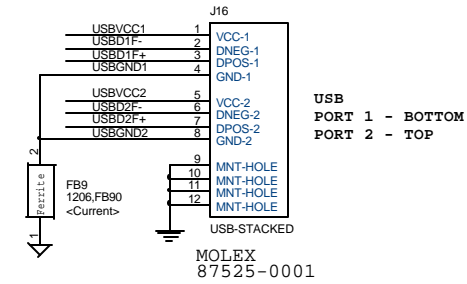
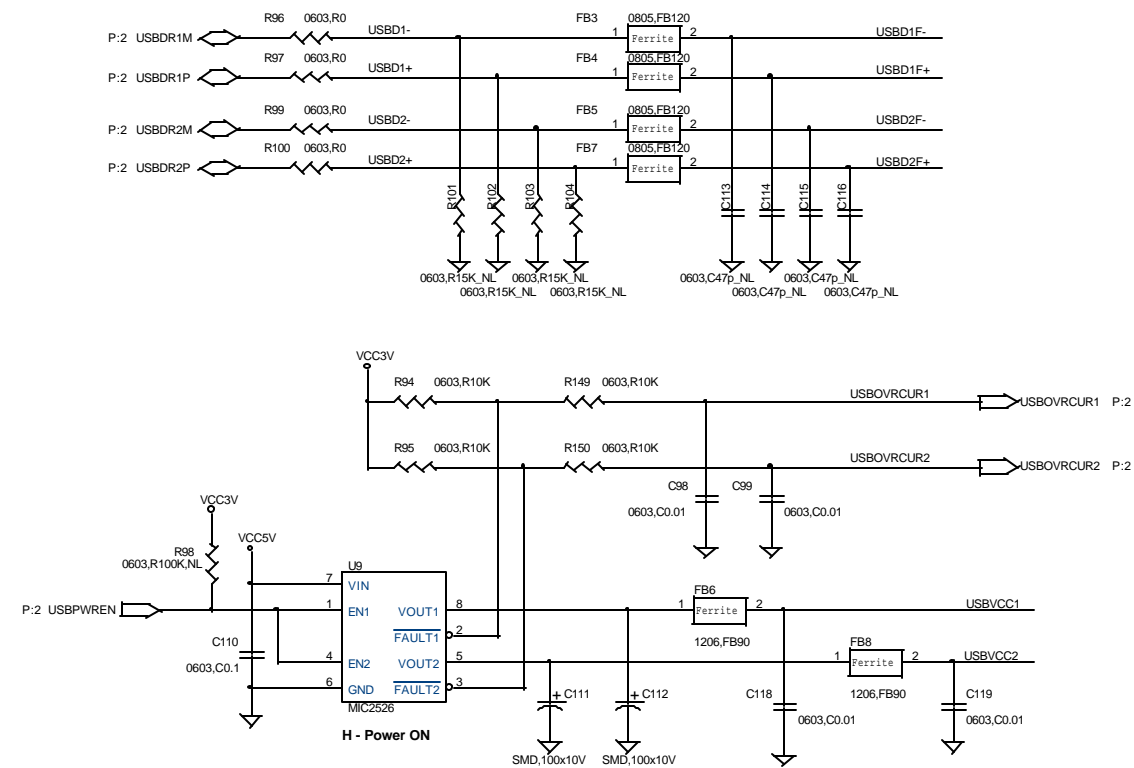


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 Palo Alto, CA, 94303
 (650) 965-3800

Title: **ISA CONNS, FLASH, BOOTSTRAP**

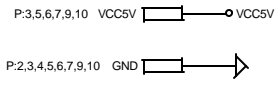
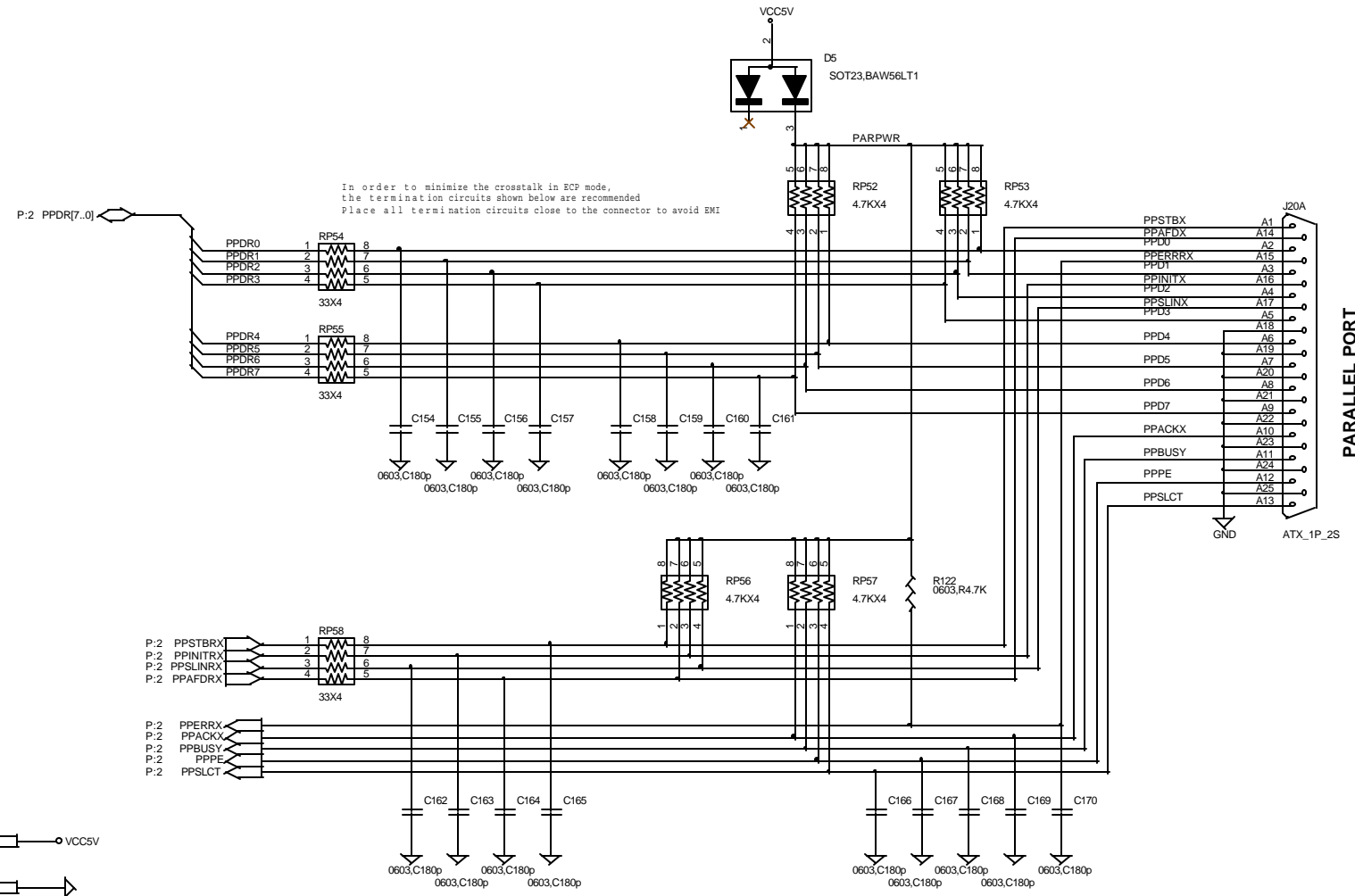
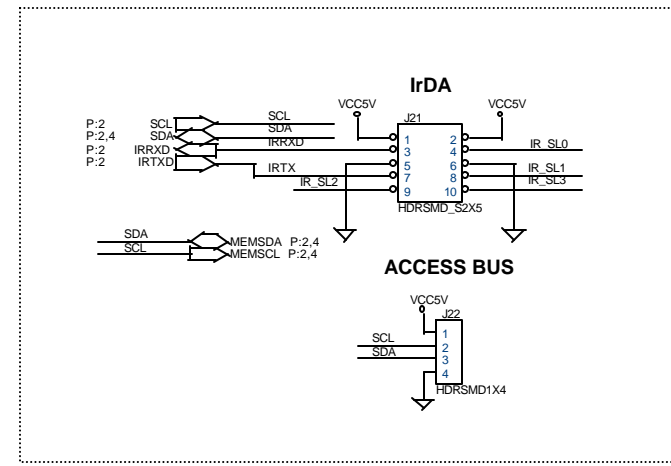
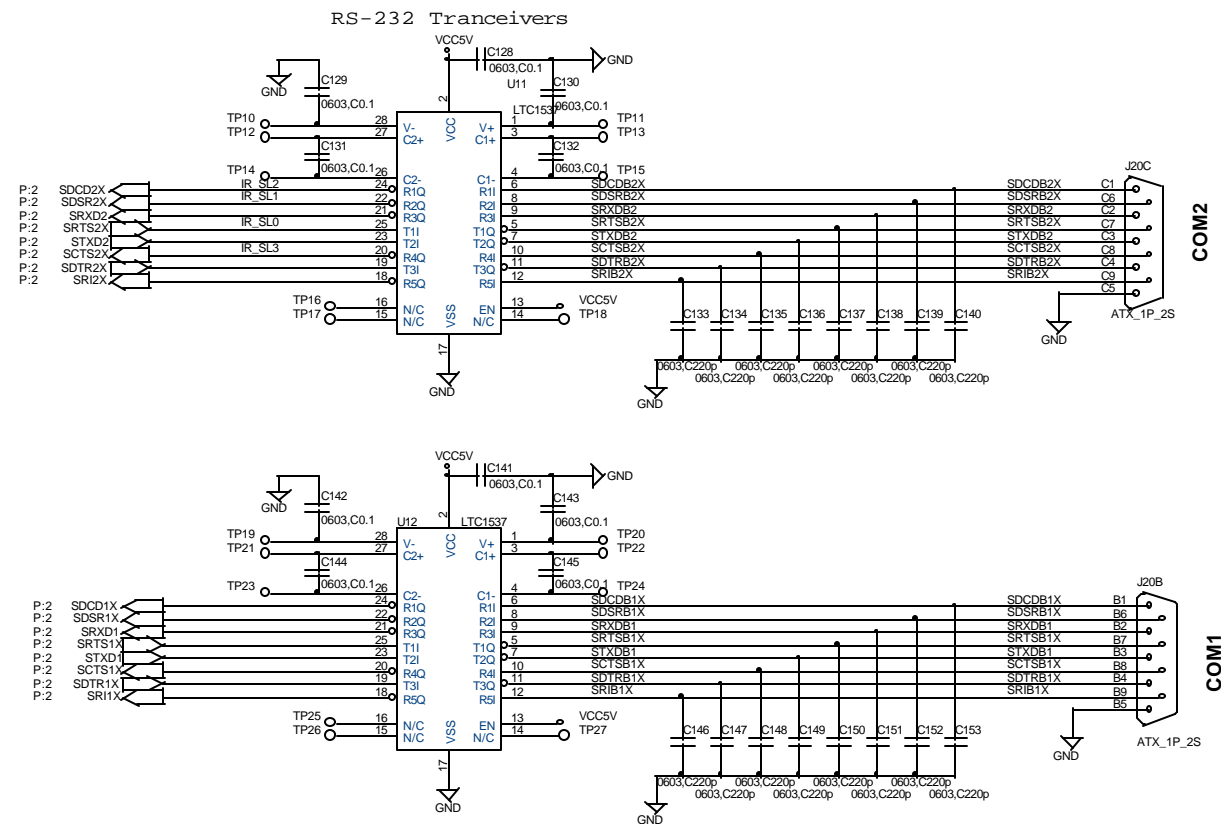
Size: C Document nr: 9000041303 ZF nr: 9400-0038-03 Rev: 3

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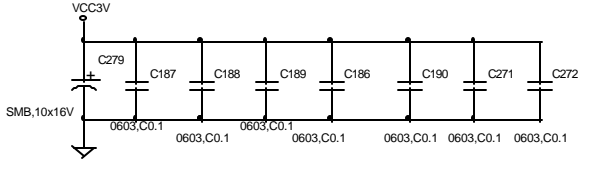
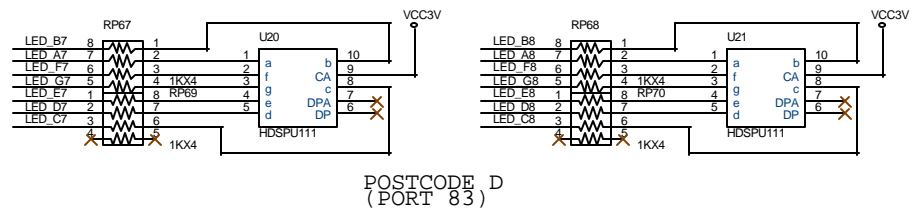
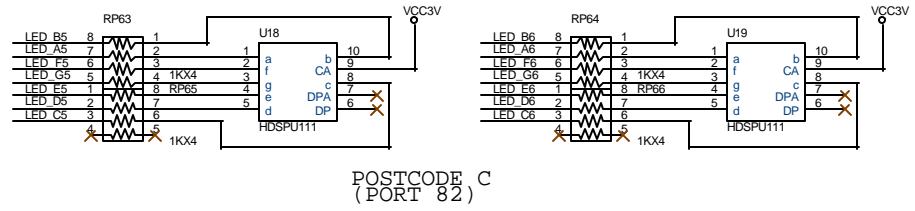
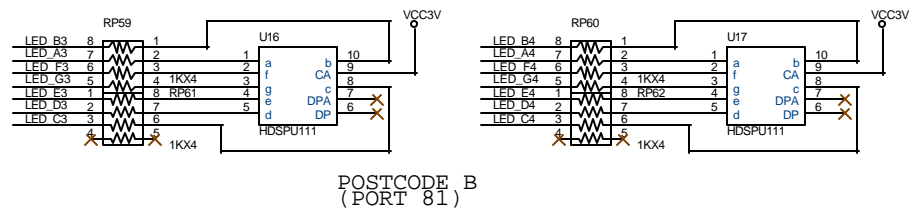
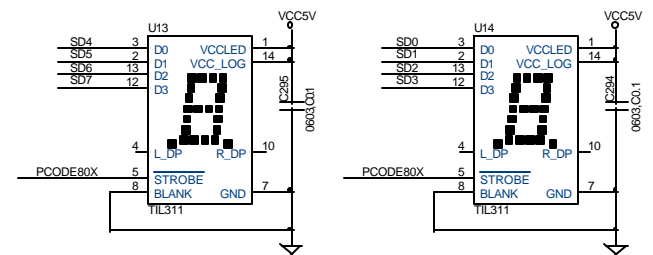
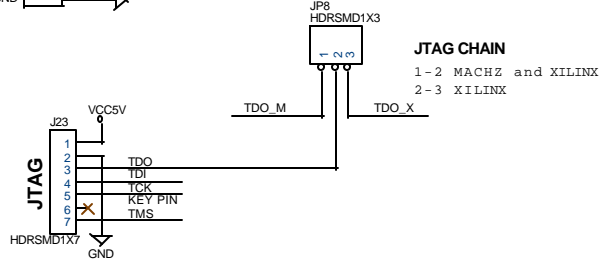
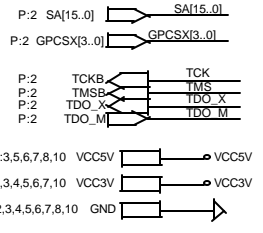
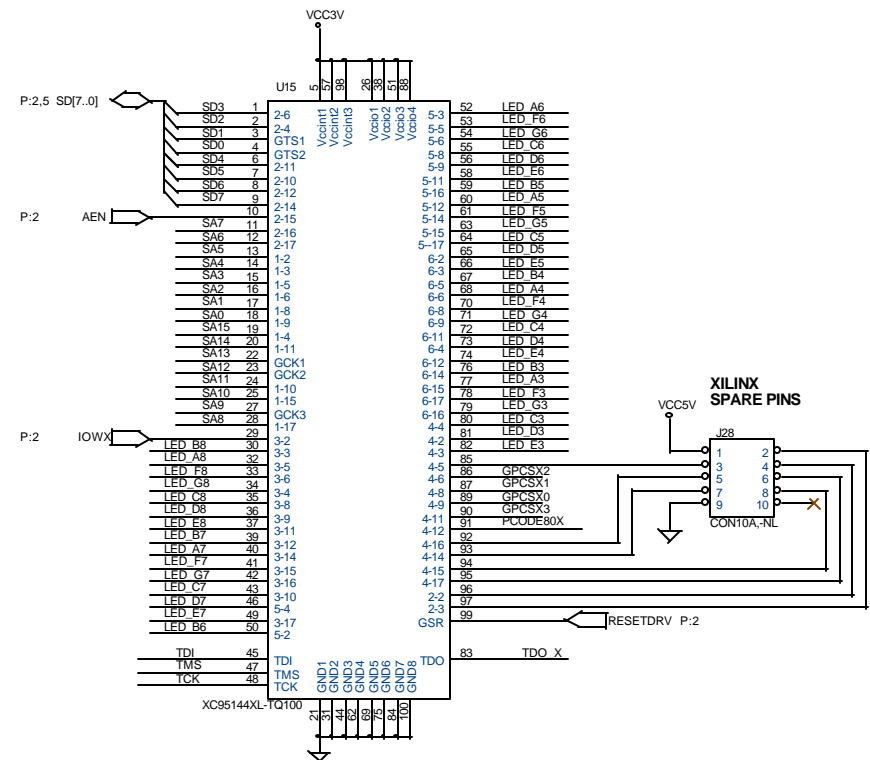


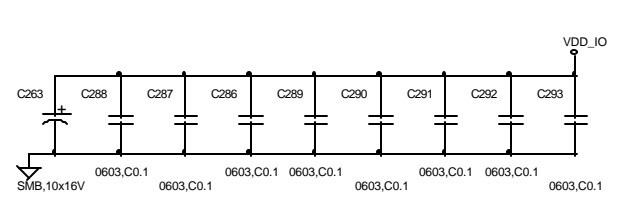
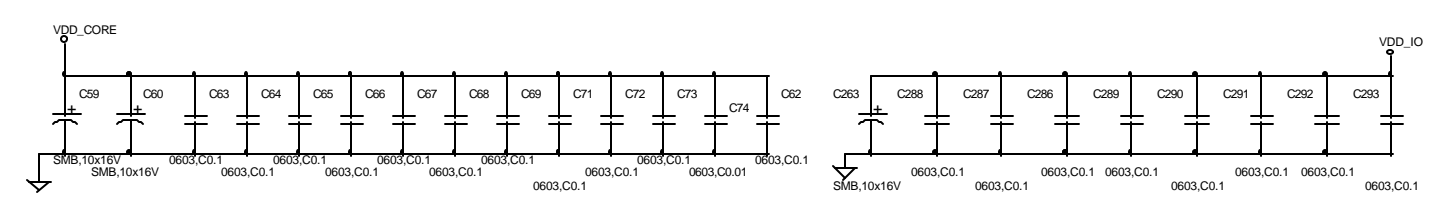
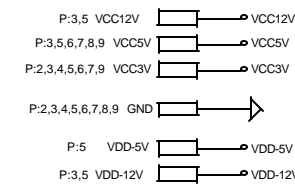
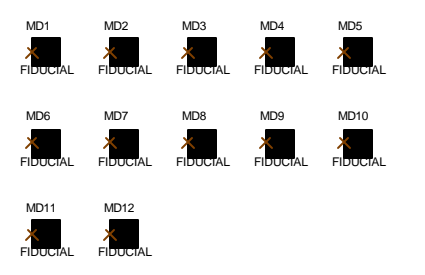
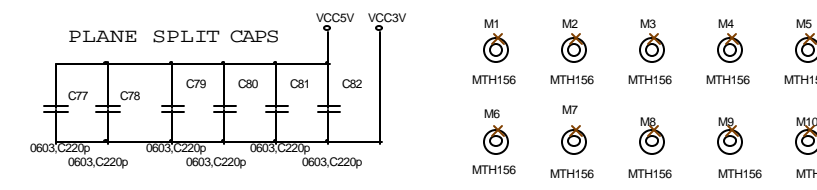
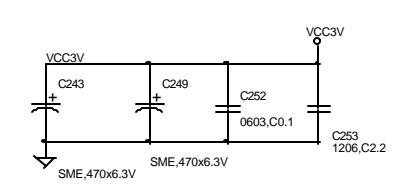
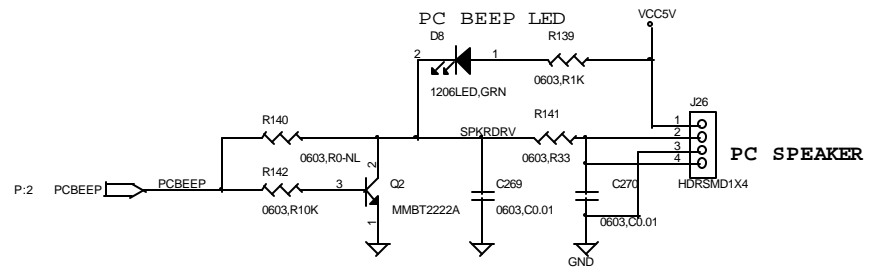
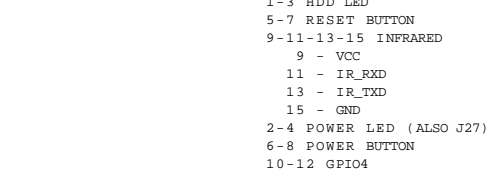
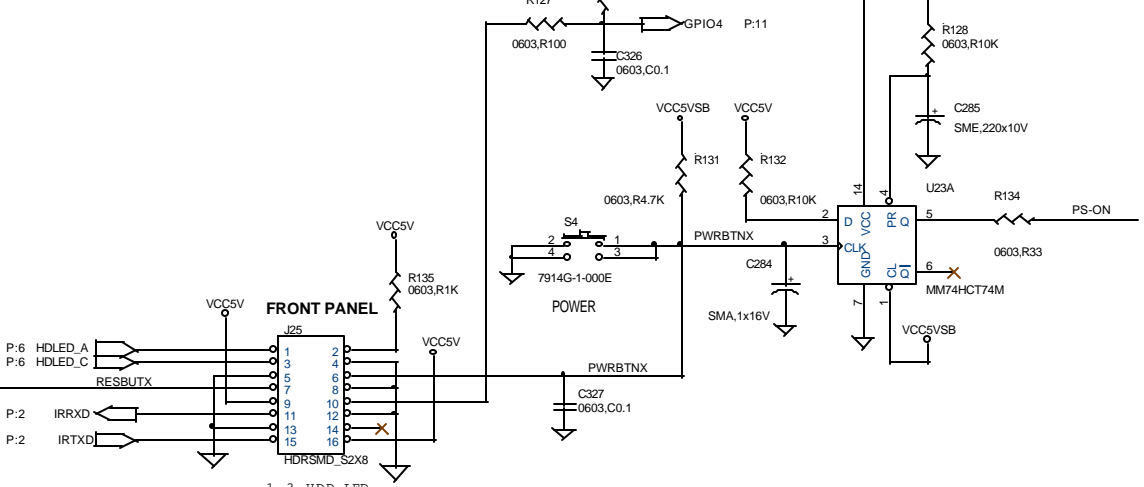
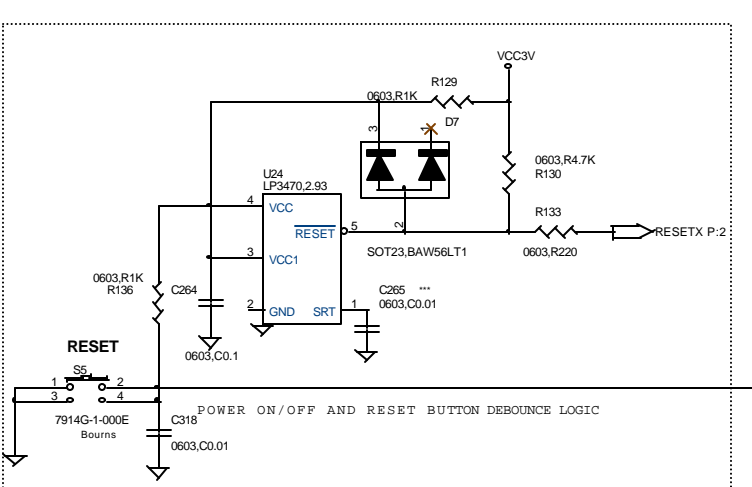
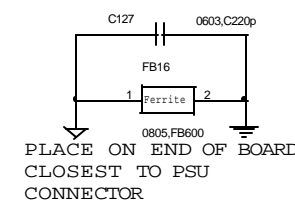
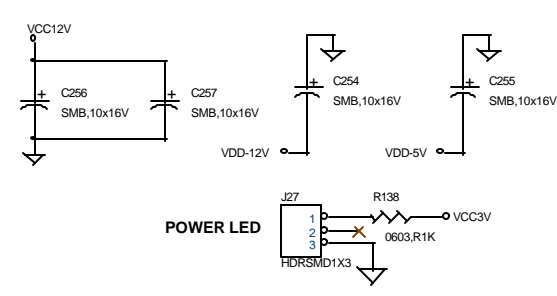
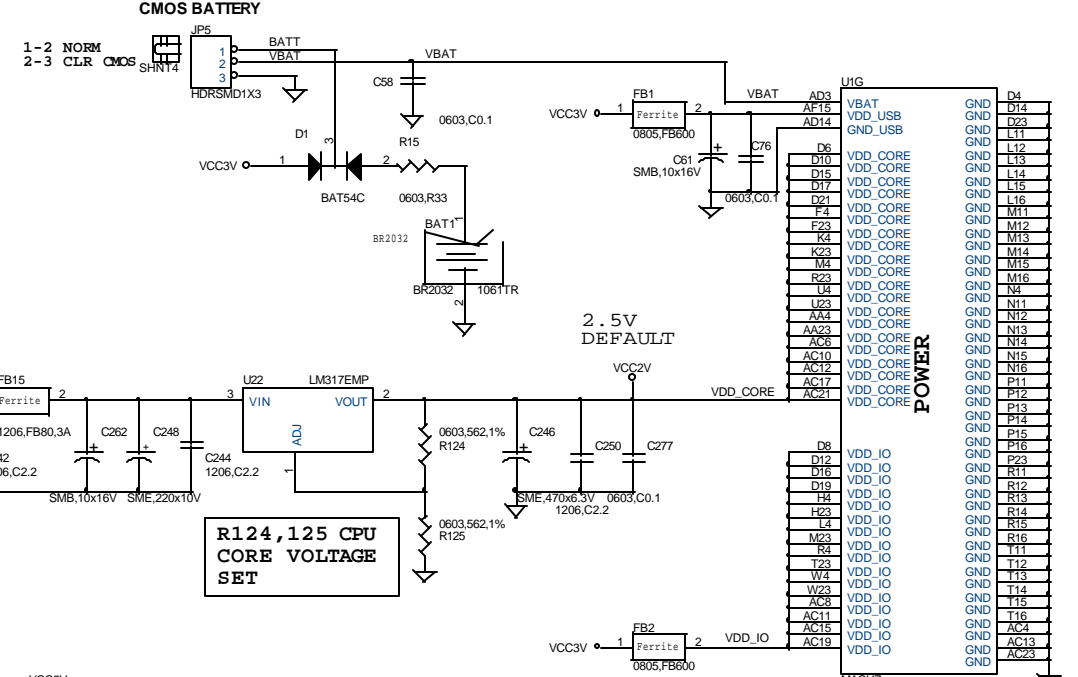
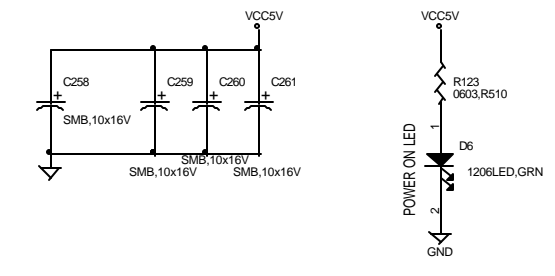
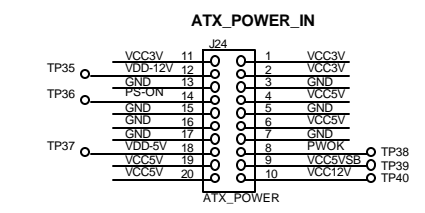
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- 8<ZDIN
- 9<SEREN_N
- 10>ZLED_1
- 11<ZACK
- 12>ZCLCK
- 13<ZRST
- 14<ZGPI0

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Title: KBD, MOUSE, FDD, USB, ZTAG			
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Title SERIAL & PARALLEL, IrDA & B			
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Title: POWER, RESET & FRONTPANEL			
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DEFAULT SETTINGS

(USING EXTERNAL CLOCKS, BIOS IN SOCKET FLASH_0 (U5),
33MHz SYSCLK AND PCICLK, 66MHz CPUCLK)

DEFAULT JUMPER SETTINGS

JP1 CLK14M SOURCE 1-2 External	JP6 DMA/PCI 3-5 and 4-6 PCI REQ2X/GNT2X ENABLED
JP2 WATCHDOG 1-2 External Source	JP7 FLASH 0-3 CS CONF 1-3 FLASHCSX0 is connected to FLASH_0 (U5)
JP3 SYSCLK SOURCE 1-2 CLK2SYS (REFER TO JP10)	JP8 JTAG CHAIN 2-3 Chain has XILINX only
JP4 PCICLK SOURCE 1-3 & 2-4 External	JP9 RTC 32 kHz INPUT 1-2 Crystal Y2
JP5 CMOS BATTERY 1-2 Battery connected	JP10 SYS and PCI CLK SPEED 1-3 and 2-4 33MHz

BOOTSTRAP DIP SWITCHES

04:0	X	(User defined)
05: Derive 14MHz from 48MHz	ON	(Using ext 14KHz)
06: Derive 32KHz from 48MHz	ON	(Using ext 32KHz)
09: Third PCI req/qrt enable	OFF	(Third PCI req/gnt Enabled)
12: boot rom width 8/16	OFF	(8 bit external ISA ROM)
16:17 1486 clk mode	OFF:ON	(2x sysclk_c)
18: front pci clk div	ON	(Divide sysclk_c by one)
19: back pci clk div	ON	(Divide sysclk_c by one)
20: back pci clock source	ON	(Use external source)
21: usb test mode enable	ON	(No USB Test)
23: BUR enable	OFF	(BUR Disabled)

ON-BOARD BOOTSTRAPS

07: 486 DLL enabled	UP	(486 DLL clock enabled)
08: 486 raw clock disabled	UP	(486 raw clock disabled)
10: SIO test mode	DOWN	(Test mode disabled)
11: int/ext bur	UP	(Use internal BUR when Ztag enabled)
13:15 1486 clk delay	TBD	(factory default)
22: zfl enable	UP	(ZF Logic Enabled)